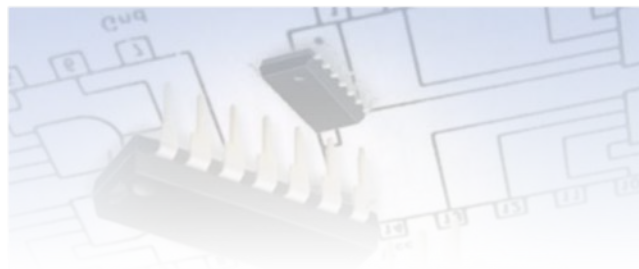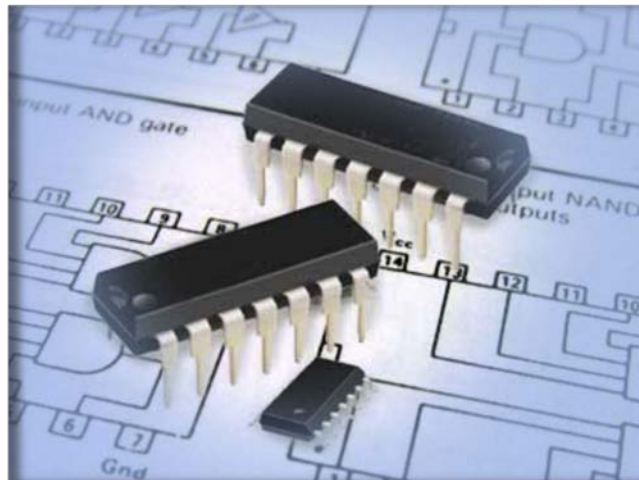# Hashemite University

Mechatronics Engineering Department

Logic and Electronics

Laboratory Manual

Experiment 1
Introduction to Combinational Logic

Objectives:

In this experiment you will investigate the logic behavior of various IC gates such as:

- 7400 Quadruple 2 input NAND gates.
- 7402 Quadruple 2 input NOR gates.
- 7404 Hex inverters.
- 7408 Quadruple 2 input AND gates.
- 7432 Quadruple 2 input OR gates.
- 7486 Quadruple 2 input XOR gates.
- To write Boolean functions in their standard Min and Max terms format.
- To simplify Boolean expressions using Karnaugh Map.

Apparatus:

This comprehensive digital –analog training system is ideal for both analog and digital circuits and contains a wealth of equipment and features. The training system contains all the peripherals needed to support your logic circuit design. Components can be connected without soldering, by simply inserting them into the breadboard. Your circuit can then be powered by the internal power supplies, signals applied if needed from the function generator and monitored on the built-in test equipment and displays.

Figure 1.1: Digital-Analog Training System

Theoretical Background:

1. Truth Tables

A truth table is a table that describes the behavior of a logic gate. It lists the value of the output for every possible combination of the inputs and can be used to simplify the number of logic gates and level of nesting in an electronic circuit.

2. Simplification

Logic functions can be complicated sometimes. In such cases we may use many tools to simplify them like: Boolean algebra theorems, De Morgan theorems or Karnaugh map. Boolean algebra theorems and De Morgan theorems will be the subject of this session while Karnaugh map will be the subject of the next session.

3. Boolean Algebra Theorems

Table 2.1 shows Boolean algebra theorems.

Associative law	$(A.B).C = A.(B.C) = ABC$
	$(A + B) + C = A + (B + C) = A + B + C$
Distributive law	$A.(B + C) = AB + AC$
	$A + (B.C) = (A + B)(A + C)$
Commutative law	$A.B = B.A$
	$A + B = B + A$
Precedence	$AB = A.B$
	$A.B + C = (AB) + C$
	$A + B.C = A + (BC)$
Single variables theorems	$AA = A$
	$A + A = A$
	$A + \overline{A} = 1$
	$A\overline{A} = 0$
	$A = \overline{\overline{A}}$

More two variables theorems	$A + AB = A$ $A + \bar{A}B = A + B$
Identity and Null operations	$A.1 = A$ $A + 1 = 1$ $A + 0 = A$ $A.0 = 0$ $\bar{1} = 0$ $\bar{0} = 1$

Table 2.1: Boolean algebra theorems.

Example 1.1 shows how to use Boolean algebra theorems in simplifying functions.

Example 1.1:

$$A(X,Y,Z) = (X + Y).(X' + Y)$$
$$= XX'+XY+X'Y+YY$$
$$= 0+Y(X+X)+Y$$
$$= Y$$

4. De Morgan's Theorems

The most important logic theorems for digital electronics are De Morgan's Theorems. These theorems state that any logical binary expression remains unchanged by applying all the following steps:

- Change all variables to their complements.
- Change all AND operations to ORs.
- Change all OR operations to ANDs.
- Take the complement of the entire expression.

In Symbols, De Morgan's theorems are stated as follows:

1. $(A.B)' = A'+B'$
2. $(A + B)' = A'.B'$

A practical operational way to look at De Morgan's Theorem is that the inversion bar of an expression may be broken at any point and the operation at that point replaced by its opposite (i.e., AND replaced by OR or vice versa). The following example shows the correct steps to apply De Morgan's theorems on a logic expression.

Example 1.2:

$$\overline{\overline{A + \overline{\overline{BC}}}}$$

$$\overline{A + (\overline{B} + \overline{C})}$$ Breaking shortest bar (AND changes to OR)

$$\overline{A + \overline{B} + \overline{C}}$$ Applying associative property to remove parentheses

$$\overline{A}.\overline{\overline{B}}.\overline{\overline{C}}$$ Breaking long bar in two places (ORs change to ANDs)

$$\overline{A}BC$$ Applying the identity $\overline{\overline{X}} = X$

5. Sum of Products & Product of Sums

Any Boolean expression can be simplified in many different ways resulting in different forms of the same Boolean function. All Boolean expressions, regardless of their forms, can be converted into one of two standard forms; the sum-of-product form and the product-of-sum forms. Standardization makes the evaluation, simplification and implementation of Boolean expression more systematic and easier.

The Sum-of-Product (SOP):

Writing functions in SOP form means that the inputs of each term are multiplied using AND function, then all terms are added together using OR function. The variables in each term are not necessarily all the variables of the function. For example, a SOP of F(A,B,C) may contain a term that contains only the variable A but not B nor C, in such case the term is not in its *standard SOP form*. *Standard SOP term* must contain all the function variables. From Boolean algebra thermos (X+X'=1), then if the term is multiplied by (X+X'), it becomes in the standard SOP form, but its value is not affected.

Example 1.3:
The following function is written in the SOP form:
F(A,B,C)=A+BC'+A'BC

The inputs to the function F are A, B and C. In each term the inputs are ANDed then all terms are ORed to form the function F.

Note that the last term A'BC contains all the inputs of the function (A, B and C), so, this term is written in standard form. But the second term BC' is not in standard form because the input A does not exist, then multiply by (A'+A). The same is done for the remaining term as follows:

 F(A,B,C)=A(B+B')(C+C')+BC'(A+A')+A'BC
F(A,B,C)=ABC+ABC'+AB'C+AB'C'+ ABC'+A'BC'+A'BC

From Boolean algebra,

(A+A=A)

then all similar terms in the equation will be reduced to one term. Now the function F becomes

F(A,B,C)=ABC+ABC'+AB'C+AB'C'+ A'BC'+A'BC

The Product-of-Sum (POS):

Writing functions in POS form means that the inputs of each term are Added together using OR function then all terms are multiplied together using AND function. The variables in each term are not necessarily all the variables of the function. For example, a POS of F(A,B,C) may contain a term that contains only the variable A but not B nor C, in such case the term is not in its *standard POS form*. *Standard POS term* must contain all the function variables. From Boolean algebra thermos (X.X'=0), then if the term is added to (X.X'), it becomes in the standard POS form, but its value is not affected.

Example 1.4:
The following function is written in the POS form:

F(A,B,C)=A.(B+C').(A'+B+C')

The inputs to the function F are A, B and C. In each term the inputs are ORed then all terms are ANDed to form the function F.

Note that the last term (A'+B+C') contains all the inputs of the function (A, B and C), so, this term is written in standard form. But the second term (B+C') is not in standard form because the input A does not exist, then add (A'.A). The same is done for the remaining term as follows:

F(A,B,C)=[A+(B.B')+(C.C')].[(B+C')+(A.A')].(A'+B+C')

F(A,B,C)=[(A+B+C).(A+B+C').(A+B'+C).(A+B'+C')].[(A+B+C').(A'+B+C')].(A'+B+C')

From Boolean algebra,

(A.A=A)

then all similar terms in the equation will be reduced to one term. Now the function F becomes

F(A,B,C)=(A+B+C).(A+B+C').(A+B'+C).(A+B'+C').(A'+B+C')

6. Minterms

Writing a function in its **minterm** format is equivalent to writing the function in its standard SOP format such that the value of the function at these terms is 1. So that if we have the truth table relating the input variables to the function F, then we can determine which cases result in F=1 and write the minterm form of the function.

Example 1.5:
Using the following truth table 1.2, write the function F in its minterm format

The function F is equal to 1 in the highlighted cases, which are the cases of 0,2,6 and 7 or A'B'C', A'BC', ABC' and ABC respectively.

The function F is written in minterm format as follows:
F(A,B,C)= A'B'C'+A'BC'+ ABC'+ ABC
Or
F(A,B,C)=∑(0,2,6,7)

	A	B	C	F
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

Table 1.2

7. Maxterms

Writing a function in its maxterm format is equivalent to writing the function in its standard POS format such that the value of the function at these terms is 0. So that if we have the truth table relating the input variables to the function F, we can determine which cases result in F=0 and write the maxterm form of the function.

Example 1.6:
Using the truth table 1.2, write the function F in its maxterm format.

The function F is equal to 0 in the un-highlighted cases above, which are the cases of 1,3,4 and 5 or (A+B+C'), (A+B'+C'), (A'+B+C) and (A'+B+C') respectively.

The function F is written in maxterms as follows:
F=(A+B+C').(A+B'+C').(A'+B+C). (A'+B+C')
Or
F(A,B,C)= Π(1,3,4,5)
Note: From Example 1.3 and 1.4, the maxterm is the complement of the minterm.

8. Karnaugh Map

The Karnaugh map (K-map) provides a systematic way of simplifying Boolean algebra expressions. This can be done without thoroughly searching the basic theorems of Boolean algebra. Instead all the possible combinations of the variables written in the standard form for **POS (product of sums) or SOP (sums of products)** are plotted in cells arranged in a rectangle or square. Adjacent cells share a redundant Boolean variable. The simplification of the original Boolean expression comes from grouping the logical one's (minterms) or 0's (maxterms). This eliminates the redundant variable and simplifies the original Boolean expression.

The circulation must be done according to the following rules:

1. A group must contain either 1, 2, 4, 8, 16…..cells.
2. Each cell in a group must be adjacent to one or more cells in the same group, but all cells do not have to be adjacent to each other.
3. Always include the most possible of 1's in a group in accordance to rule (1).
4. Each 1 on the K-map must be included in at least one group. The 1's in a group can be included in another group as long as the overlapping groups include non-common 1's.

Example 1.7 shows how to use the K-map to simplify functions.
Example 1.7:
Simply the following function using K-map

F(A,B,C)=A'B+ABC'+B'C'

In order to use the K-map the function should be written in its min or maxterms format.

F(A,B,C)=A'BC+A'BC'+ABC'+AB'C'+A'B'C'

F(A,B,C)=∑(0,2,3,4,6)
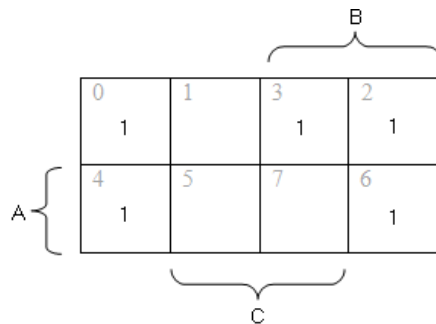
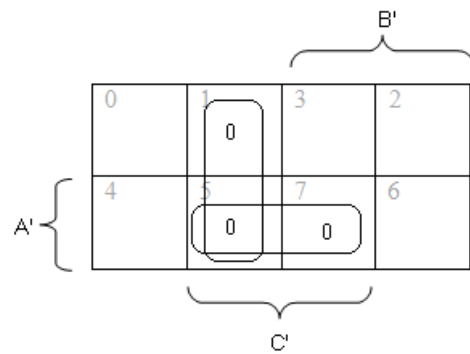To write the function as simplified SOP then circle the 1's in K-map
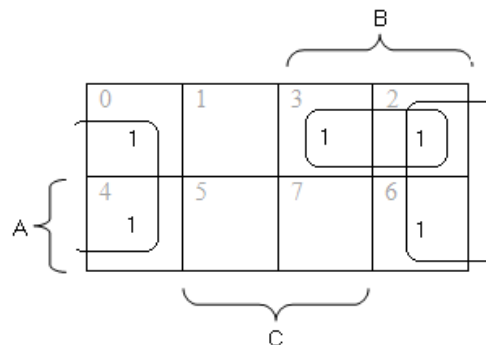
From K-map, F(A,B,C)=C'+BA'

F is written in maxterm as follows

F(A,B,C)= ∏(1,5,7)

To write the function as POS then circle the 0's in K-map

From K-map, F(A,B,C)=(A'+C').(B+C')

Procedure:

1- Ask your instructor to give you the digital logic IC's, after making your design on labwork sheet.
2- Insert the IC's in the digital training system breadboard, then referring to the datasheet connect your design
3- After being sure your circuit is connected correctly, turn on the digital training system power.

Discussion and Analysis:

1- How many inputs, and outputs in your design?
2- If you decide to use maxterm instead of minterm simplification , is your design will be the same ? explain.

Experiment 2
Introduction to Sequential Logic

Objectives:

In this experiment you will be able to:

- Design a sequential logic circuit using D-Flip-flop.
- Implement the designed circuit.
- Design a sequential logic circuit using JK-Flip-Flop.
- Implement the designed circuit.

Apparatus:

This comprehensive digital –analog training system is ideal for both analog and digital circuits and contains a wealth of equipment and features. The training system contains all the peripherals needed to support your logic circuit design. Components can be connected without soldering, by simply inserting them into the breadboard. Your circuit can then be powered by the internal power supplies, signals applied if needed from the function generator and monitored on the built-in test equipment and displays.

Theoretical Background:

So far we have implemented digital circuits whose outputs depend only on its inputs in experiment 1,Such circuits are called **combinational logic circuits** and do not depend on the state of the output. Another type of digital circuits is presented in this session and called the **sequential logic circuits**.

The next output Q+ (at time t+) of these circuits depends upon the present one Q (at time t) as well as upon the Boolean input variables. Sequential circuits have a memory of what has previously happened or in other words sequential circuits contain combinational circuits to which storage elements are connected to form a feedback path. The inputs for the sequential circuits together with the present state of the output determine the binary value of the next output.

- **Memory Elements**:

The basic memory elements in sequential circuits are called latches and flip-flops. These devices -constructed from NAND and NOR gates- are bistable, this means that the latch or the flip-flop output can exist for an indefinite time in one of two stable states.

By convention the output of a flip-flop is called "Q". We set a flip-flop by changing "Q" to logical 1. We reset the flip-flop by changing "Q" to a logical 0.

Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

There are four main types of flip-flops which are shown in Figure 2.1
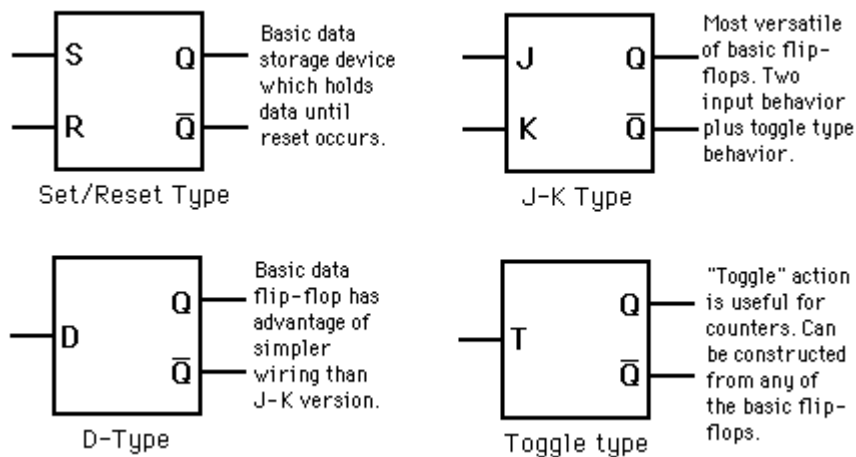

Figure 2.1: Types of flip flops.

- **D Flip Flop:**

The D stands for "data"; this flip-flop stores the value presented at on the data line. It can be thought of as a basic memory cell. The D flip-flop tracks the input, making transitions that match those of the input D. The D flip-flop output "Q" tries to follow the input D but cannot make the required transitions unless it is enabled by a rising or falling edge of a clock.

Table 2.1: D flip flop truth table.

Input D	Clock	Next state Q^+	
0	↑	0	Reset
1	↑	1	Set

And the characteristic equation for the D flip-flop is:

$$D = Q(t) = Q^+$$

(2.1)

The internal construction of D flip flop is shown in Figure 2.2. Figure 2.3 represents the time diagram of a D flip flop.
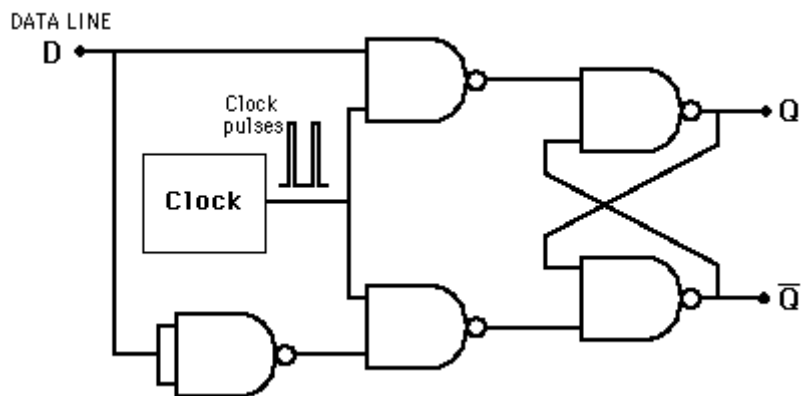
Figure 2.2: Internal construction of D flips flop.
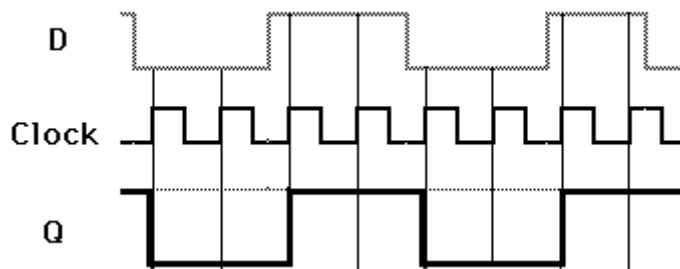
Figure 2.3: Time diagram of D flip flops.

- **Logic Circuits Design Using D-Flip Flop.**

The best way to explain the procedure of designing using D flip flop is through an example.

Example 2.1

Design using D flip flop a logic circuit that opens a door when a switch is turned on and the door is closed. And closes the door when the switch is turned off and the door is opened.

The door is an output Y(Door closed=0)
The switch is an input X (turned on=1)
Solution:

Step one: Derive circuit state diagram.

The state diagram representing the problem in hand is shown in Figure 2.4.
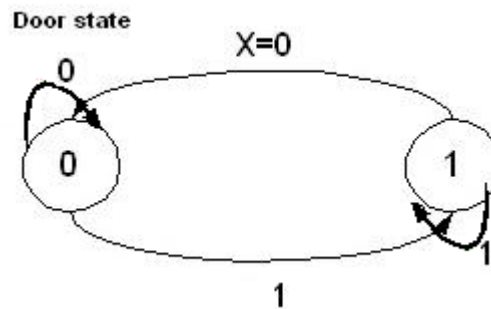
Figure 2.4: Example 2.1 state diagram.

Step two: Create state table.

The un-hashed columns in Table 2.2 represent the state table obtained from the state diagram.

Table 2.2: Example 2.1 state and excitation table.

Input X	Current state Q	Next state Q^+	D	Y
0	0	0	0	0
0	1	0	0	0
1	0	1	1	1
1	1	1	1	1

Step three: Create circuit excitation table.

This is shown by the hashed columns in Table 2.2. These columns are derived using Equation 2.1.

Step four: Construct K-maps for the flip-flop input (D) and the output (Y).

In this example the primary output Y is the same as the flip flop output Q which is the same as the input of the D flip flop, so only one K-map is enough to find the input D and the primary output Y. Observe Figure 2.5 and notice that the inputs of the k-map are the input X and the current state of the flip flop.
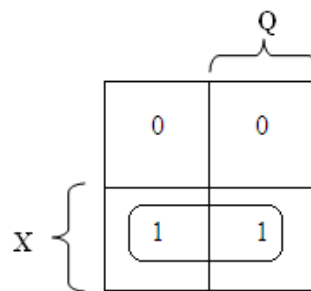
Figure 2.5: Example 2.1 K-map.

According to the K-map above

D=X

Then the input of the D flip flop will be connected directly to the switch X (only for this example) and it does not depend on the current state of the flip flop Q.

Step five: Implement the logic circuit.

The logic circuit for this application is shown in Figure 2.2.
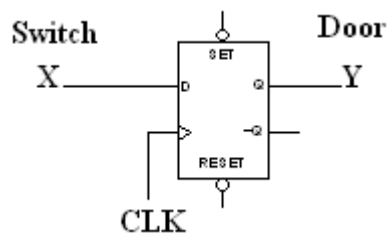

Figure 2.6: Logic circuit for Example 2.1.

Example 2.2

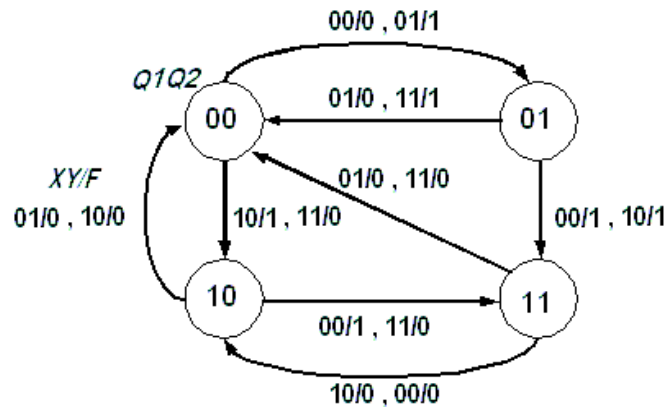Design a logic circuit using D flip flop for the state diagram shown in Figure 2.7.

Figure 2.7: State diagram for Example 2.2.

Table 2.3: State and excitation table for Example 2.2.

Input X	Input Y	Current state Q1	Current state Q2	Next state $Q1^+$	Next state $Q2^+$	Output F
0	0	0	0	0	1	0
0	0	0	1	1	1	1
0	0	1	0	1	1	1
0	0	1	1	1	0	0
0	1	0	0	0	1	1
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	1	0	1
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	0	0	1
1	1	1	0	1	1	0
1	1	1	1	0	0	0

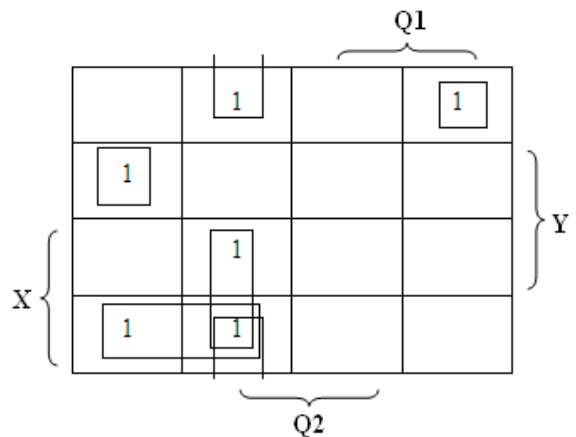Since D1= Q1$^+$, we can obtain the following K-map from Q1$^+$ column.
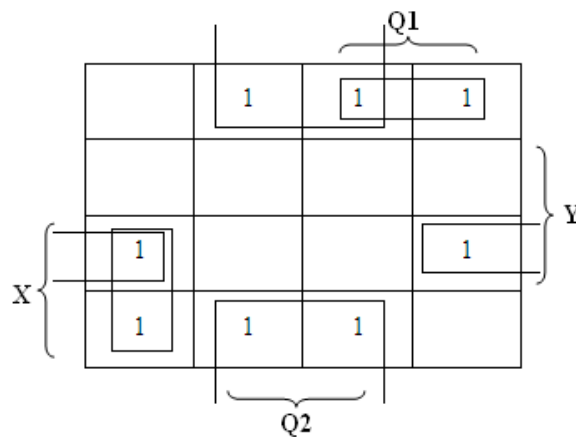
D1= Q1$^+$ = Y'Q2 + XQ1'Q2' + XYQ2' + X'Y'Q1

Since D2= Q2$^+$, we can obtain the following K-map from Q2$^+$ column.
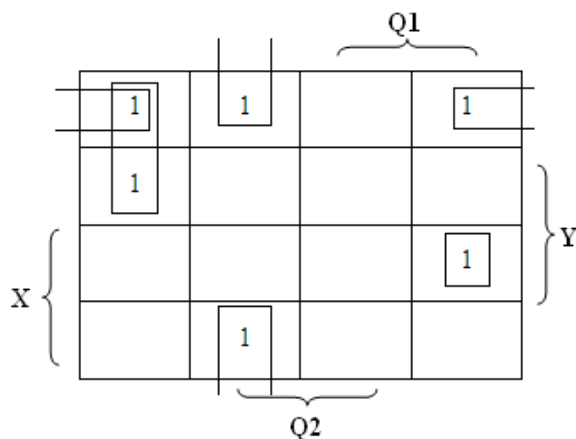
D2= Q2$^+$ = XYQ1Q2' + X'Q1'Q2' + Y'Q1'Q2 + X'Y'Q2'

The following K-map is obtained from the primary output F column.

F = XQ1'Q2 + XY'Q1' + Y'Q1'Q2 + X'YQ1'Q2' + X'Y'Q1Q2'

The logic circuit for Q1 and Q2 are shown in Figure 2.8. The logic circuit of the primary output F is omitted for simplicity.
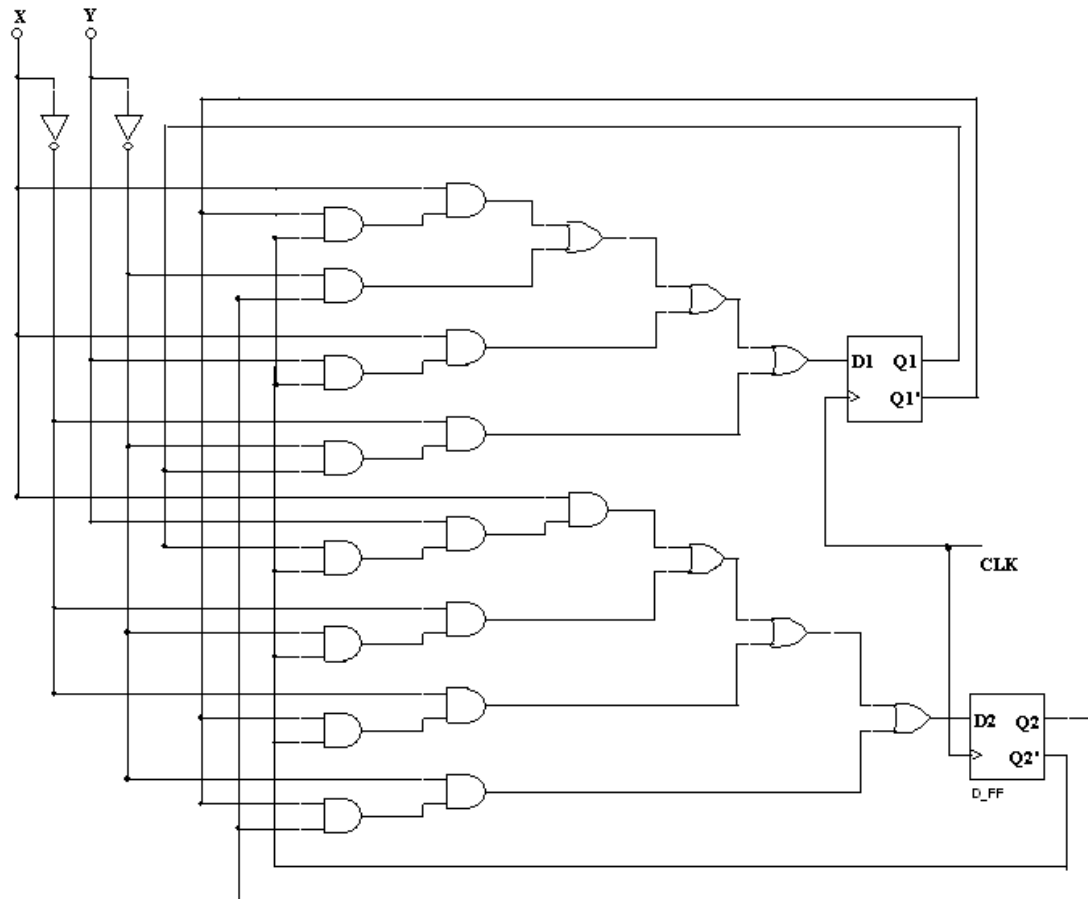

Figure 2.8: Logic circuit for Example 2.2.

Procedure:

1- Ask your instructor to give you the digital logic IC's, after making your design on labwork sheet.
2- Insert the IC's in the digital training system breadboard, then referring to the datasheet connect your design
3- After being sure your circuit is connected correctly, turn on the digital training system power.

Discussion and Analysis:

1- How many inputs you need in your design.
2- If you design your logic circuit using D-flip flop, change your design to use JK flip flop. Is it easier than using D-flip flop?

Experiment 3
Decoders & Counters

Objectives:

- To use decoders to implement logic functions.
- To implement decoders using 74LS138 and 74LS139 ICs.
- To design digital counter circuits using JK-Flip-Flop.
- To implement counter using 74LS193 IC.

Apparatus:

This comprehensive digital –analog training system is ideal for both analog and digital circuits and contains a wealth of equipment and features. The training system contains all the peripherals needed to support your logic circuit design. Components can be connected without soldering, by simply inserting them into the breadboard. Your circuit can then be powered by the internal power supplies, signals applied if needed from the function generator and monitored on the built-in test equipment and displays.

Theoretical Background:

- **Decoders**

Discrete quantities of information are represented in digital system with binary codes. A binary code of N bits is capable of representing up to 2^N distinct combinations.

A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its input and indicates the presence of that code by a specified output level. In its general form, a decoder has n input lines to handle N bits and from one to 2^N output lines to indicate the presence of one or more N-bit combinations.

Consider a 2*4 decoder, it has 2 inputs and 4 output lines. The truth table for a 2*4 decoder is shown in Table 3.1.

Table 3.1: Truth table of 2*4 decoder.

Inputs		Outputs			
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Each combination of inputs (A & B) activates only one output line. From the truth table,
D0=A'.B'   **D1=A'.B**
D2=A.B'   **D3=A.B**
Because the active output in each case is indicated by a HIGH signal (one), this type of decoders is called active HIGH decoders. On the other hand, if the active output is indicated by a LOW signal (zero), the decoder is called active LOW decoders. The decoder circuit is shown in Figure 3.1 and its symbol is shown in Figure 3.2.
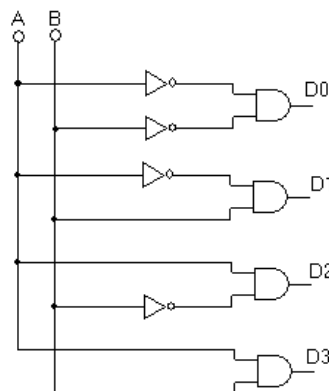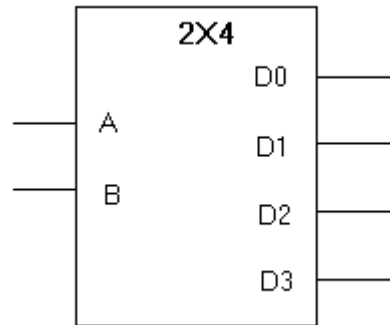

Figure 3.1: 2*4 decoder logic circuit.

Figure 3.2: 2*4 decoder circuit symbol.

An active LOW decoder IC of N inputs has 2^N output, but can be used to generate a single active HIGH output by using NAND as illustrated by the following example:

Example 3.1:

Design a logic circuit using an active LOW 2*4 decoder, such that:

$F(A,B)=\sum(1,2)$

where F is an active HIGH function.

Solution:

The function F is HIGH when the input combination is AB' or A'B. In other words, when the output lines D1 or D2 (of the active LOW decoder) are LOW.

The logic circuit needed to build the function F is shown by Figure 3.3.
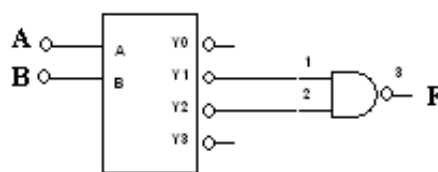

Figure 3.3: Logic circuit needed to solve Example 3.1.

- **Counter**

Circuits for counting events are frequently used in computers and other digital systems. Since a counter circuit must remember its past states, it has to possess memory. Flip-flops are introduced and connected to make a counter. The number of flip-flops used and how they are connected determine the number of states and the sequence of the states that the counter goes through in each complete cycle.

Counters can be classified into two broad categories:
   a. Synchronous counters
   b. Asynchronous counters

a- Synchronous Counters:

In synchronous counter all clocks of flip-flops are connected to the same clock signal. Thus, all flip-flop outputs change state at precisely the same moment. Table 3.2 shows the states of a 2-bit counter. Each state is an increment to its previous state by 1, which means that the counter is an up counter. It is clear from the table that the first flip-flop (FF0) toggles at the clock edge (either rising or falling), according to this, this part of the counter is implemented using T flip-flop and its input is always at high logic. The second flip-flop (FF1) toggles if the output of FF0 is 1. Then this part of the counter is also implemented with T flip-flop but with its input connected to the output of the previous flip-flop.

Table 3.2: 2-bit counter.

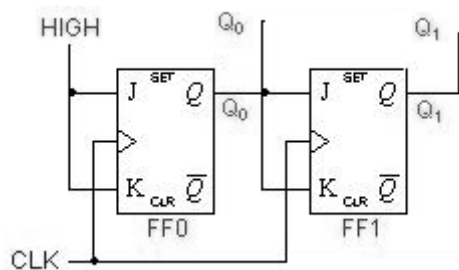| Q1	Q0
0	0
0	1
1	0
1	1

Figure 3.4: 2-bit synchronous counter.

Example 3.2
Design a logic circuit that counts from 0 to 4 then back to 0 only if an input signal is 1. Use synchronous counter.

Solution:

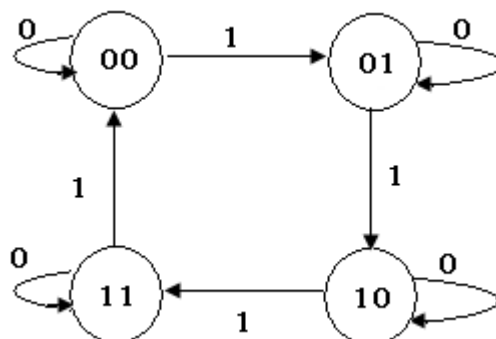**Step one:** Figure 8.5 shows the state diagram.

Figure 3.5: Example 3.2 state diagram

Step two and three: The state and excitation tables are shown in table 3.3.

Table 3.3: State and excitation tables of Example 3.2.

Current state		Input	Next state		Flip flop 1		Flip flop 0	
Q1	**Q0**	**U**	**Q1$^+$**	**Q0$^+$**	**J1**	**K1**	**J0**	**K0**
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Step four: Construct K-maps for each flip-flop inputs (J and K)
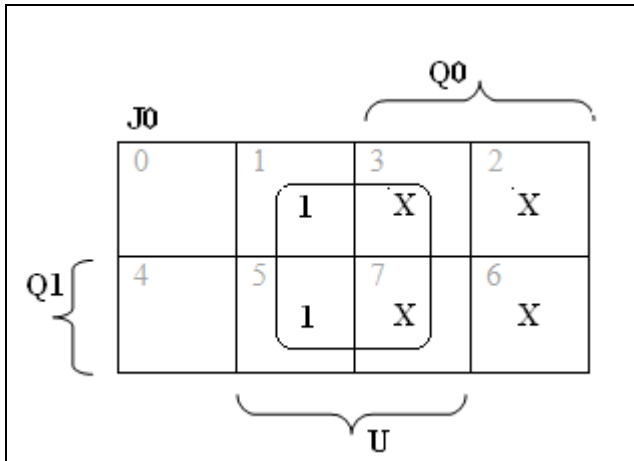
Figure 3.6: K-map for J0 in Example 3.2.

J0=U
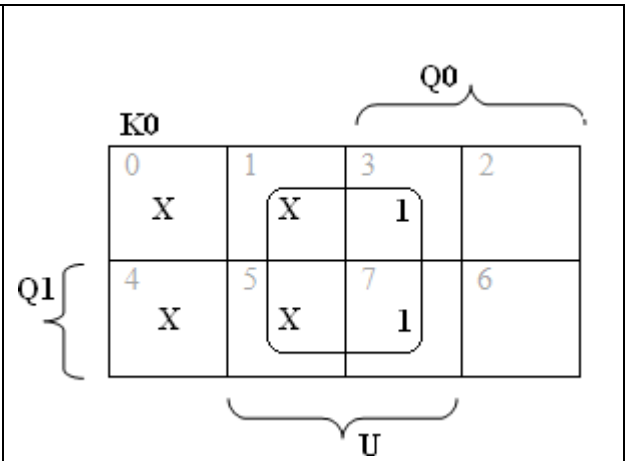

Figure 3.7: K-map for K0 in Example 3.2.

K0= U

Notice that even though the implementation is with JK flip-flop the result is that K0=J0 then it is a T flip-flop
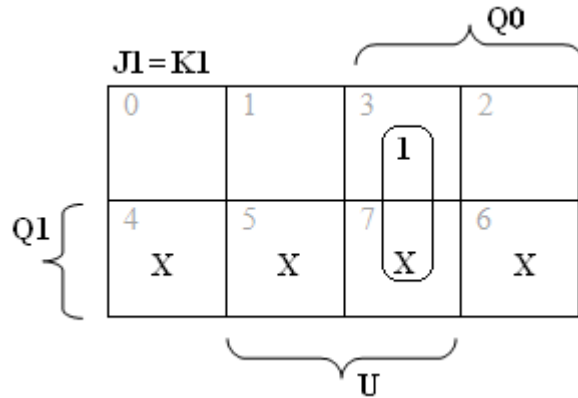
Figure 3.8: K-map for J1=K1 in Example 3.2.

J1=K1=Q0.U

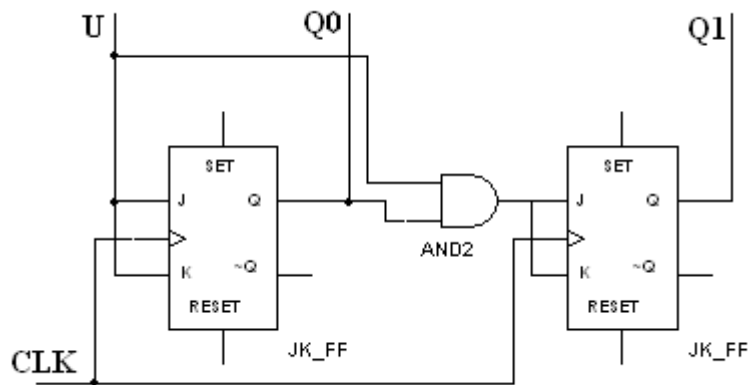**Step five:** The logic circuit is implemented in Figure 3.9.

Figure 3.9: The logic circuit for Example 3.2

Procedure:

For **synchronous counter**, the design procedure is the same procedure of designing using flip-flops, starting from the state diagram and ending with the logic circuit.

Discussion and Analysis:

Design a 4-bit logic circuit that counts from 2 to 7 , only if an input signal is 1. Use synchronous counter. Hints: you have to use decoder to stop counting at 7.

Experiment 4
Diode Types and Characteristics

Objectives:

In this experiment you are expected:
- To be familiar with basic properties of diodes, Zener diodes and LED.
- To study the characteristics of the diode by investigating the I-V curve.
- To study the characteristics of the Zener diode by investigating the I-V curve.
- To differentiate between regular diode and Zener diode properties.

Apparatus:

Dc supply

Function Generator

Digital multimeter

Oscilloscope

Theoretical Background:

A diode is a semiconductor device consists of single pn-junction with nonlinear i-v characteristics. Diode permits current conduction in only one direction; from the anode (the positive terminal) to the cathode (the negative terminal) forming one way switch see figure 1. Its operation falls in one of three regions:
1. Forward biased.
2. Reverse biased.
3. Reverse breakdown (failure).

Zener diode is a special type of diodes designed to operate in the reverse breakdown region, where it maintain a constant voltage drop across its terminals.

LEDs -or Light Emitting Diodes- are another type of diodes that emits light when forward biased. The color emitting from each diode depends on the materials of the pn-junction.

Procedure:

Part1: Forward and Reverse Voltages of Diodes

Use the DMM to measure the voltages in table 4.1. Set the DMM to the "diode testing" option.

Technical hints:

- Anode and cathode of diodes are shown in figure 4.1
- To measure the forward voltage place the positive lead of the DMM on the anode
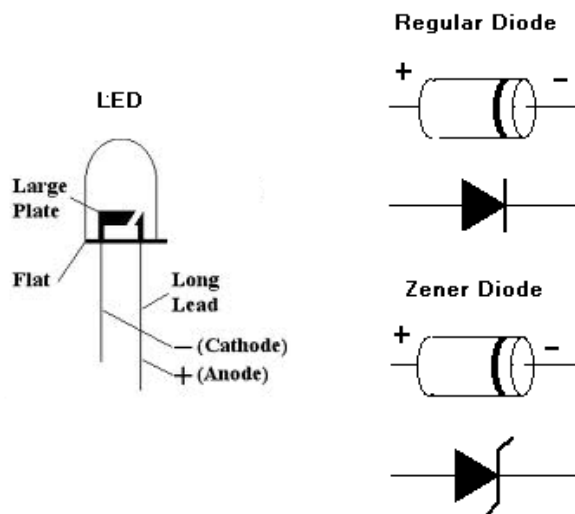- To measure the reverse voltage place the positive lead of the DMM on the cathode

Figure 4.1

Table 4.1

Diode type	Forward voltage	Reverse voltage	Observation
Regular diode			
Zener diode			
LED (color1)			
LED (color2)			

Part2: Diode Characteristics
  a. Forward biasing
    1. Connect the circuit in figure 4.2.
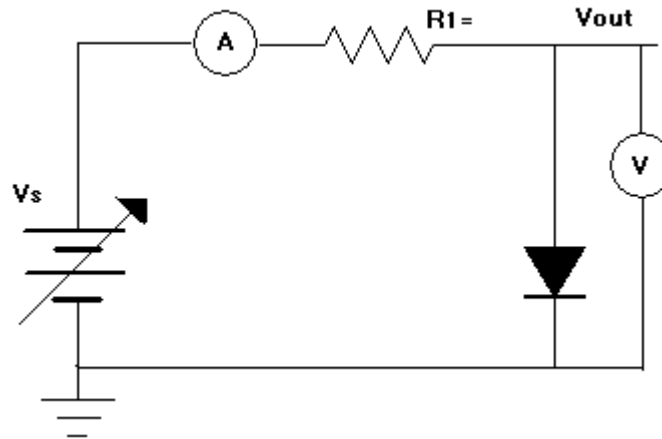   2. Measure V_{out} and I_D and fill in table 4.2.

Figure 4.2

Table 4.2:

Vs (V)	Forward voltage V_{out} (V)	Forward current I_D (A)
0		
0.5		
1.0		
1.5		
2.0		
2.5		
3		
4		
5		

b. Reverse biasing

1. Connect the circuit in figure 4.3.
2. Measure V_{out} and I_D and fill in table 4.3.
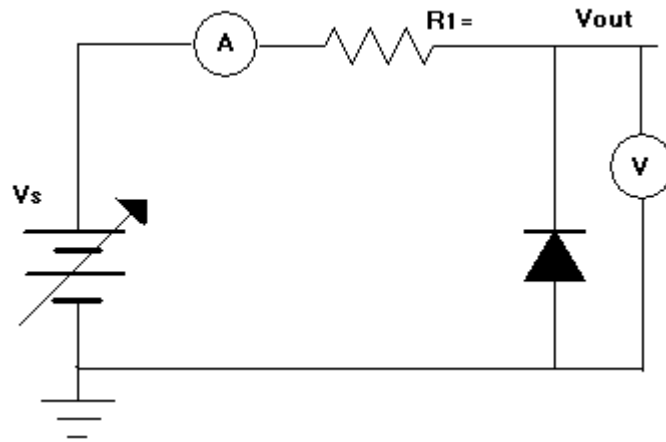
Figure 4.3

Table 4.3

Vs (V)	Reverse voltage V_{out} (V)	Reverse current I_s (A)
1		
2		
3		
4		
6		
8		
10		

c. Characteristic curve

Connect the circuit in figure 4.4. Set the oscilloscope on the (XY measurement). Observe the result, and write down the values of :

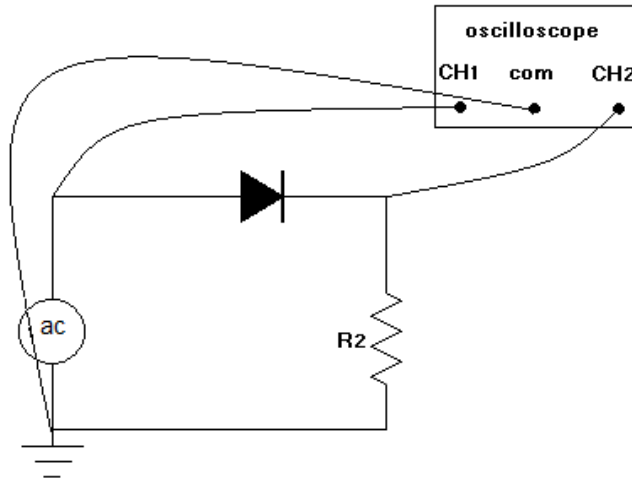V_D =_____

I_s =_____

Figure 4.4

Technical hints:

- R2 must be a multiple of 10KΩ for current scaling
- Invert channel 2 of the oscilloscope to obtain a positive reading of the current

Part3: Zener Characteristics

Repeat **Part 2** but first replace all diodes in the circuits with Zener diodes then fill in the following tables:

a.   Forward biasing

Table 4.4:

Vs (V)	Forward voltage V_{out} (V)	Forward current I_D (A)
0		
0.5		
1.0		
1.5		
2.0		
2.5		
3		
4		
5		

    b.   **Reverse biasing**

Table 1.5

Vs (V)	Reverse voltage V_{out} (V)	Reverse current I_s (A)
1		
3		
5		
7		
9		
11		
15		

    c.   **Characteristic curve**

V_z =_____

I_s =_____

Discussion and Analysis:

Part1: Forward and Reverse Voltages of Diodes

1. Fill in table 1.1 with your observations.

Part2: Diode Characteristics

2. In table 1.2, the output voltage reached a constant value. What is this value? And what does it represent?
3. What is the purpose of using R1 in the circuit of figure1.1?
4. Sketch the result you obtain from the circuit in figure 1.4. On your sketch, show the values of V_D and I_s.
5. Based on your result; dose ohm's law apply to the diodes?
6. What would it cost to obtain the breakdown voltage of a diode?

Part3: Zener Characteristics

7. In table 1.4, the output voltage reached a constant value. What is this value? And what does it represent?
8. Does the behavior of the Zener diode differ from that of a regular diode in the forward biased region?
9. Compare the results you obtained in table 1.5 (reverse biased Zener diode) to the results in table 1.3 (reverse biased regular diode).
10. Sketch the result you obtain from the circuit in figure 1.4 for the Zener diode. On your sketch, show the values of V_D ,V_Z and I_s.

Experiment 5
Diodes Applications

Objectives:

In this experiment you are expected:

- To implement clipper circuits.
- To implement clamper circuits.
- To implement two types of diode rectification circuits half-wave and full-wave rectifiers.
- To implement a voltage regulation circuit using Zener diodes.

Apparatus:

Dc supply

Function Generator

Digital multimeter

Oscilloscope

Theoretical Background:

Important applications of diode are wave-shaping circuits that either limit portions of a signal (clipper) or shift the dc voltage level (clamper).

Clipper circuits are used to eliminate portion of a signal that are above or below a specified level.

Clamper circuits shifts the entire signal voltage by dc level. The output is an exact replica of the input waveform, but with different dc level.

A common application of diode circuits are rectifiers. A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction.

Rectifier can be constructed using diode circuits and there are two types:

1. Half-wave rectifier.
2. Full-wave rectifier.

Another application of diodes circuits are voltage regulators. Voltage regulator is a circuit used to maintain a steady voltage across a load which otherwise may vary according to the change of the input voltage (line regulation) or the change of the load impedance (load regulation).

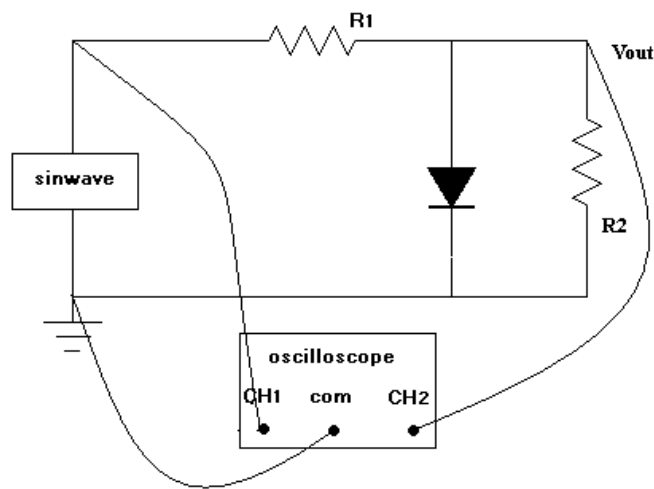## Procedure:

Part1: Clippers

1. Connect the circuit in figure5.1.

Figure 5.1

2. Consult your lab supervisor to get the correct sitting of the sinwave and the value of the resistors.
3. Plot the input and output signals on the oscilloscope monitor. (make sure that both channel has the same ground)
4. Do the needed measurements to complete table 5.1

Table 5.1

Experimental		Theoretical	
V_{max}	V_{min}	V_{max}	V_{min}

Part2: Clampers
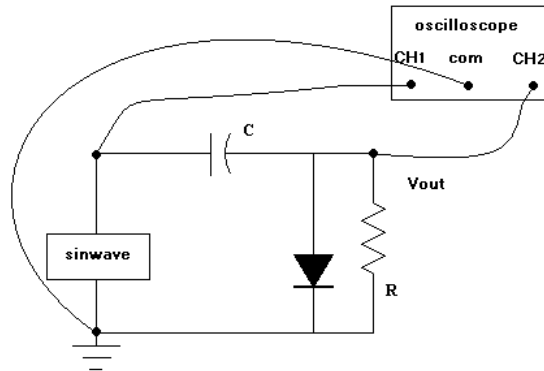
1. Connect the circuit in figure5.2.

Figure 5.2

Technical hints:

- Make sure in clamper circuit that the positive terminal of the electrolytic capacitor is connected to the cathode of the diode, or the negative terminal of the electrolytic capacitor is connected to the anode of the diode.
- The only design constraint in clamper circuit is that the period $2\pi RC$ be five times larger than the period of the input waveform.

2. Consult your lab supervisor to get the correct sitting of the sinwave and the value of the resistors.
3. Plot the input and output signals on the oscilloscope monitor. (make sure that both channel has the same ground)
4. Change the input signal into a squarewave. Consult your supervisor.
5. Do the needed measurements to complete table 5.2.

Table 5.2

	V_{max}	V_{min}	waveform
Input 1 sinewave			
Output 1			
Input 2 Squarewave			
Output 2			

Part3: Half-Wave Rectifiers

a. Unfiltered half-wave rectifier
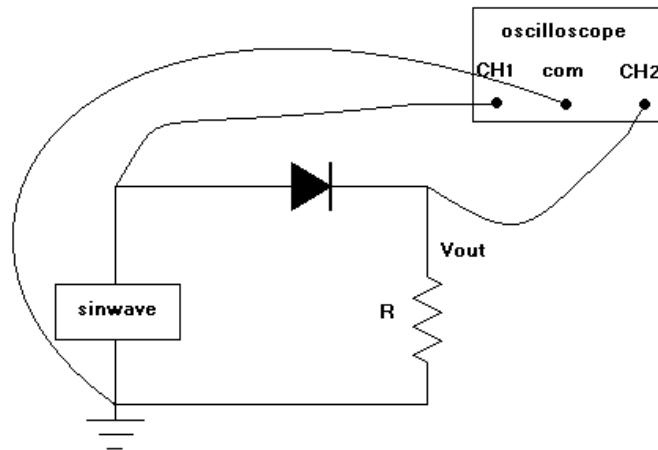
5. Connect the circuit in figure5.3.

Figure 5.3

6. Consult your lab supervisor to get the correct sitting of the function generator and the value of R.
7. Plot the input and output signals on the oscilloscope monitor. (make sure that both channel has the same ground)

b. **Filtered half-wave rectifier**
   1. For the circuit in figure 5.3, connect a capacitor in parallel with the resistor to get a circuit similar to figure 5.4.
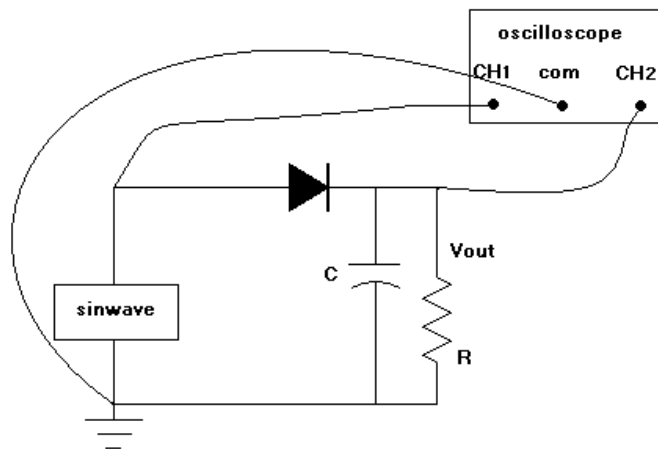

Figure 5.4

Technical hints:
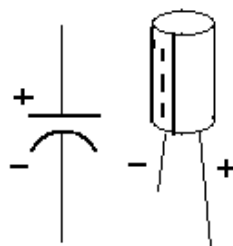
- Make sure to connect the capacitor with the proper polarity. See figure 5.5

Figure 5.5

2. Plot the input and output signals on the oscilloscope monitor. (make sure that both channel has the same ground)
3. Use the oscilloscope to measure the ripple voltage V_r=_____.

Part4: Full-Wave Rectifier

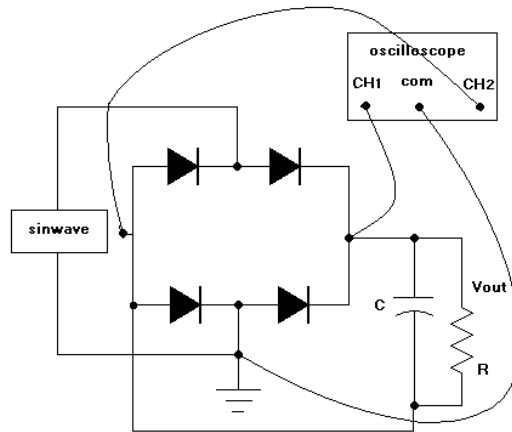6. Connect the circuit in figure5.6.

Figure 5.6

Technical hints:

- In this case the output is a **deference voltage** and is measured as illustrated in the next steps.

7. Connect the oscilloscope as shown in figure 5.6 then invert channel 2.
8. Add the signal in both channels (by this you subtracted channel 2 from channel 1 and founded the deference voltage).
9. Observe the result.
10. Measure the ripple voltage V_{r1} =_____.
11. Increase the capacitor value and measure the ripple voltage V_{r2} =_____.

Part5: Voltage Regulators
a. **Line regulation**.

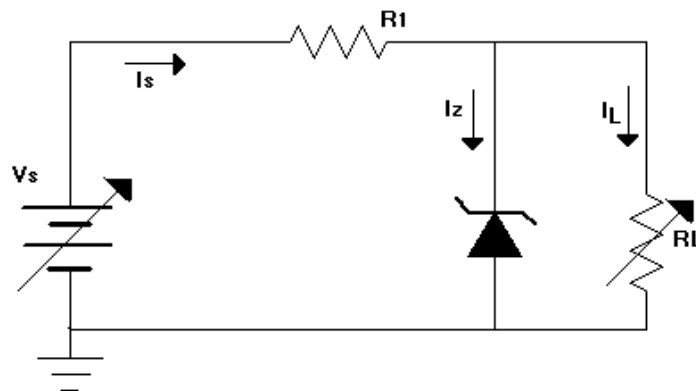1. Connect the circuit in figure 5.7 use the values in table 5.3

Figure 5.7

2. Measure V_L and V_1 and fill in table 5.3

Table 5.3

Vs (V)	measured		calculated		
	V_L(V)	V_1 (V)	I_s	I_Z	I_L
2					
4					
6					
8					
10					
RL=2.2KΩ	R1=220Ω		VR=		

b. Load regulation

1. For the circuit in figure 5.7 use the values in table 5.4.
2. Measure V_L and V_1 and fill in table 5.4.

Table 5.4

R_L (Ω)	measured		calculated		
	V_L(V)	V_1 (V)	I_s	I_Z	I_L
1.0K					
620					
470					
270					
100					
V_s=6V	R1=220Ω		VR=		

Discussion and Analysis:

Part1: Clipper

1. Sketch the output waveform of the circuit in figure5.1
2. Assume that the diode is ideal then complete table5.1.
3. Is there a difference between the experimental and theoretical values? Give one good reason for that.
4. Sketch the output waveform of the circuit in figure5.1 if the diode polarity is inverted.
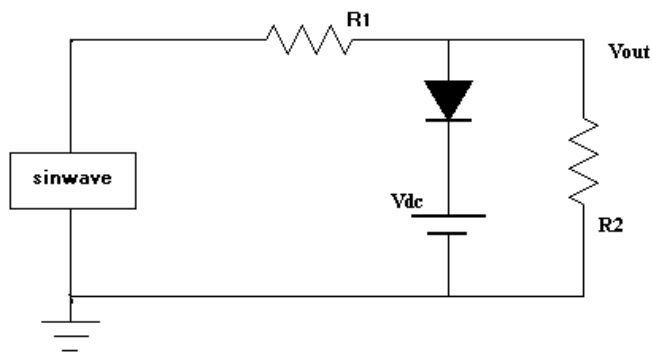5. Sketch the output wave form of the circuit in figure5.8. Is this circuit considered as a clipper?

Figure 5.8

Part2: Clamper

6. Include table 5.2 with your report showing the waveforms of the signals.
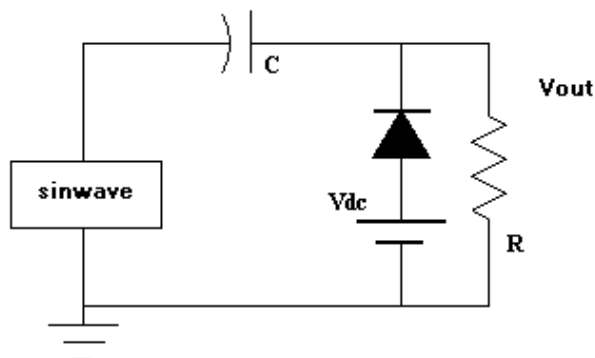7. Sketch the output waveform of the circuit in figure5.9?

Figure 5.9

8. Construct a clamper circuit to obtain the waveform in figure 5.10. Assume that $V_\gamma=0.8$
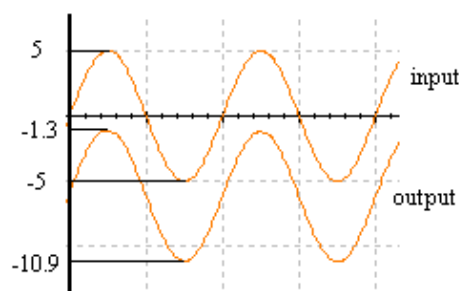

Figure 5.10

Part3: Half-Wave Rectifier

1. Sketch the output waveform of the circuit in figure5.3
2. Assume that the diode is ideal then complete table5.2. Show the equations you used.
3. Is there a difference between the experimental and theoretical values of V_{max}. give one good reason for that.
4. Sketch the output waveform of the circuit in figure5.3 if the diode polarity is inverted.
5. Sketch the output waveform of the circuit in figure 5.4
6. Calculate the output average voltage $V_{ave} = V_p/\pi - (V_\gamma/2)$.
7. Calculate the ripple percentage $r = V_r/V_{ave}$.
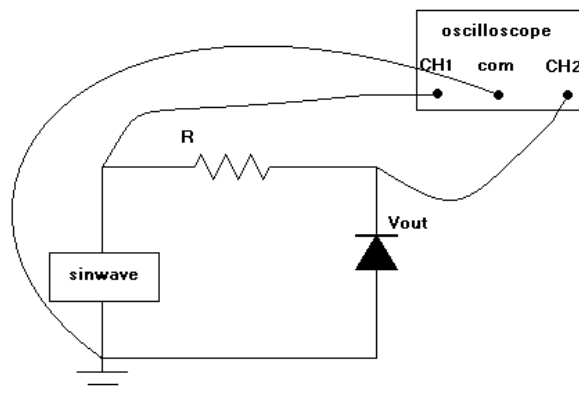8. Sketch the output wave form of the circuit in figure5.11. Is this circuit considered as a rectifier?

Figure 5.11

Part4: Full-Wave Rectifier

9. Sketch the output waveform of the circuit in figure 5.6?
10. What is the effect of increasing the capacitor value on the ripple voltage? Which capacitor is better to use?

Part5: Voltage Regulators

11. Calculate I_s, I_L, I_Z and fill in table 5.3
12. Calculate the line regulation $VR = \Delta V_{out}/\Delta V_{in} * 100\%$
13. Calculate I_s, I_L, I_Z and fill in table 5.4
14. Calculate the load regulation $VR = (V_{nl} - V_{fl})/V_{fl} * 100\%$
15. What is the purpose of using R_1?
16. For the circuit in figure 2.6, the load is 0.9A and must be operated at a constant voltage in the range of (8-9V),) chose a suitable Zener diode then calculate the minimum value of R_1. Include the datasheet of the Zener diode you've chosen with your report.
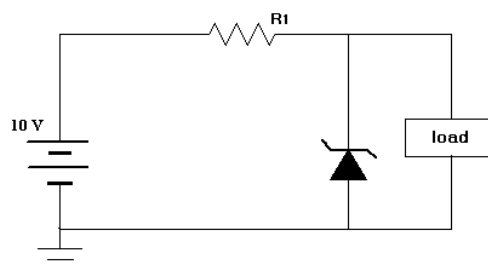

Figure 5.12

Experiment 6
Bipolar Junction Transistor

Objectives:

In this experiment you are expected:

- To experimentally distinguish between the types of Bipolar Junction Transistor (BJT) npn and pnp.
- Determine the terminals and material of a npn BJT using DMM.
- To experimentally obtain the characteristics of the npn BJT

Apparatus:

Dc supply

Function Generator

Digital multimeter

Oscilloscope

Theoretical Background:

The bipolar junction transistor (BJT) contains two pn junctions, so it has three terminals. The basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

BJT has three regions of operation; Active region, Saturation region and Cutoff region. If a BJT is to be used as an amplifier it must be biased to operate in the Active region, where the output current is proportional to the input voltage.

If the BJT is to be used as electrical switch (ON-OFF control circuits); it is biased to operate in the Saturation region (ON state, where the current is constant) or in the Cutoff region (OFF state where the current is zero).

Procedure:

Part1: Transistor Testing

Figure 6.1 shows the electrical symbol of pnp and npn transistors and figure 6.2 shows a physical transistor. Follow the next steps to find the type of the transistor (npn or pnp) and assign its terminals (base 'B', collector 'C' and emitter 'E').
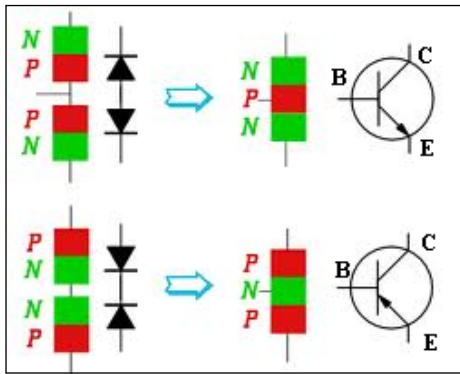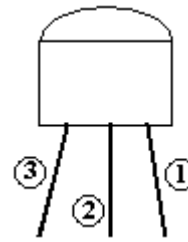

Figure 6.1

Figure 6.2

1. Write down the number written on the back of your transistor_____.
2. Label the terminal of the transistor as in figure 6.2.
3. Set the selector of the DMM on the diode option.
4. Connect the positive and negative leads of the DMM to the BJT terminals as specified in table 6.1. Record the DMM reading each time you test the terminals.

Table 6.1

Step	Positive terminal of the DMM connected to:	Negative terminal of the DMM connected to:	DMM reading
1	Terminal 1	Terminal 2	
2	Terminal 2	Terminal 1	
3	Terminal 1	Terminal 3	
4	Terminal 3	Terminal 1	
5	Terminal 2	Terminal 3	
6	Terminal 3	Terminal 2	
	Observation : npn/pnp **Note that the emitter-base voltage is slightly higher than the collector-base voltage.**		

Part2: **Transistor Parameters and DC Load Line**
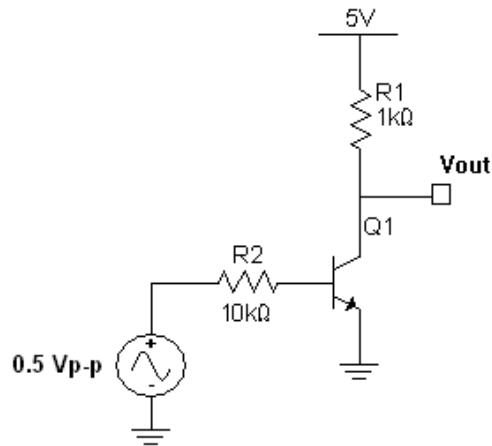
1. Connect the circuit in figure 6.3.

Figure 6.3

2. Measure the values in table 6.2

Table 6.2

parameter	measured	calculated	Error%
V_C			
V_B			
V_E			
I_{CQ}			
I_{BQ}			
I_{EQ}			
V_{CEQ}			
V_{BEQ}			
Calculate the dc current gain β_{dc}:			

Part3: **Transistor Switch**

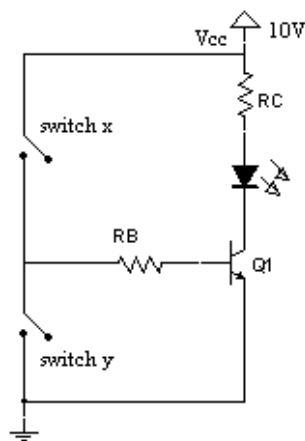1. Connect the circuit in figure 6.4.

Figure 6.4

2. Consult your lab supervisor to get the correct values of the resistors.

Warning: both switches should NOT be closed at the same time.

3. Close the switches as illustrated in table 6.3 and do the needed measurement

Table 6.3

parameter	Switches state	
	x open y closed	y open x closed
V_C		
V_B		
V_E		
LED state On/off		
Transistor region of operation		

Discussion and Analysis:

Part1: Transistor Testing

1. Based on the data in table 6.1 what is the type of the transistor?
2. Assign the emitter, collector and base of the transistor based on the measurements in table 6.1.

Part2: Transistor Parameters and DC Load Line

1. Analyze the circuit in figure 6.3 and fill the values you calculated in table 6.2. Include table 6.2 with your report.
2. Calculate the percentage error in each parameter.
3. Calculate the current gain $\beta dc = IC/ IB$
4. Write down the load line equation. VCE = f(IC).
5. Plot the load line and assign the measured Q-point on it

Experiment 7
Operational Amplifier

Objectives:

In this experiment you are expected:
- To experimentally deal with OP-Amps.

Apparatus:

Dc supply

Function Generator

Digital multimeter

Oscilloscope

Theoretical Background:

An operational amplifier (op-amp) is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals.

The circuit symbol for an op-amp is shown by figure 7.1, where,

V+: non-inverting input

V-: inverting input

Vout: output

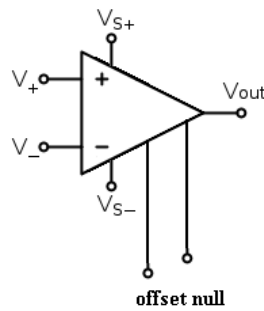Vs+: positive power supply

Vs-: negative power supply

Figure 7.1

Ideal operational amplifier has the following specifications:

1. Infinite input resistance.
2. Zero output resistance.
3. Infinite common mode rejection ratio (CMRR).
4. Zero input current and input voltage offsets.

Ideal op-amp does not really exist. This will cause some practical issues.

Technical hints:

- The positive and negative power supply must be connected properly. See the datasheet of the IC.
- For a zero input voltage, the output of a *real* op-amp is not zero.
- The solution to this problems is to null the amplifier to compensate for this offsets. See figure 7.2.
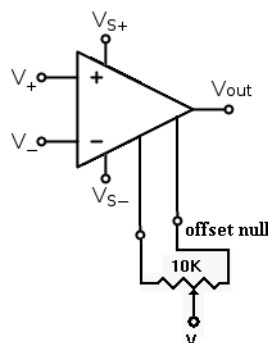

Figure 7.2

Op-amp can be implemented in circuits in different configuration to perform different tasks such as:

1. Inverting amplifier.
2. Non-inverting amplifier
3. Summing amplifier.
4. Differential amplifier.
5. Instrumentation amplifier
6. Integration amplifier

Procedure:

Part1: Op-amp Nulling
1. Implement the circuit shown in Figure 7.3
2. Switch on the power supplies.
3. While Vin=0 V and the switches are open, measure the output voltage V$_{out}$=_____.
4. While Vin=0 V, adjust the potentiometer till the output voltage equals 0V.
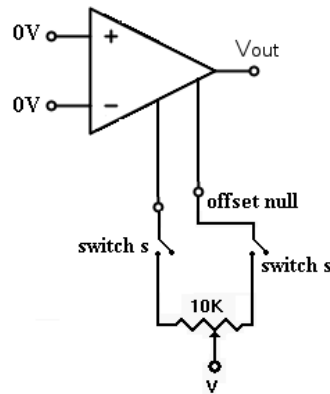5. Note that this procedure must be done each time you implement an op-amp circuit.

Figure 7.3

Part2: Inverting Amplifier
1. Implement the circuit shown in figure 7.4.
2. Consult your lab supervisor to get the values of the resistors.
3. Switch on the power supplies.
4. While V$_{in}$=0 V, Adjust the potentiometer to null the op-amp.
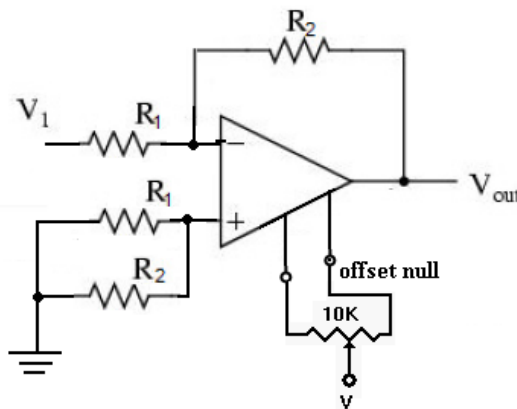5. Adjust the value of V$_{in}$ and fill in table 7.1

Figure 7.4

 Part3: Summation Amplifier
1. Implement the circuit shown in figure 7.5.
2. Consult your lab supervisor to get the values of the resistors.
3. Switch on the power supplies.
4. While V_{in}=0 V, Adjust the potentiometer to null the op-amp.
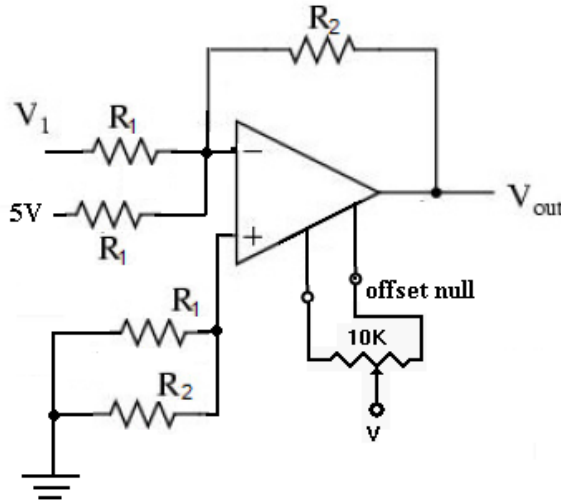5. Adjust the value of V_{in} and fill in table 7.1

Figure 7.5

Part4: Difference Amplifier
1. Implement the circuit shown in figure 7.6
2. Consult your lab supervisor to get the values of the resistors.
3. Switch on the power supplies.
4. While V_{in}=0 V, Adjust the potentiometer to null the op-amp.
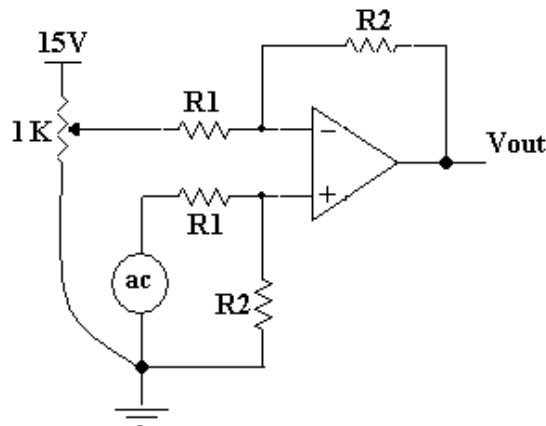5. Adjust the value of V_{in} and fill in table 7.1

Figure 7.6

Table 7.1

V_{in} (V)	V_{out}		
	Inverting amplifier	Summation amplifier	Difference amplifier
8			
7			
6			
5			
4			
3			
2			
1			
0			
-1			
-2			
-3			
-4			
-5			
-6			
-7			
-8			

Discussion and Analysis:

Part1: Op-amp Nulling
1. If the op-amp is ideal what is the value of V_{out} while the switch is open?

Part2: Inverting Amplifier
2. Plot the output voltage of the inverting amplifier versus the input voltage.
3. From your plot, find the slope of the curve. What does the slope represent?
4. Calculate the gain of the inverting amplifier and compare it with the gain you obtained experimentally.

Part3: Summation Amplifier
5. On the same plot in step 2, plot the output voltage of the summing amplifier versus the input voltage.
6. From your plot, find the slope of the curve. What does the slope represent?

Part4: Difference Amplifier
7. Plot the output voltage of the deference amplifier versus the input voltage. Calculate the slope.
8. In all circuits of this experiment, what happens to the output when the input voltage is more than 6V? Explain.
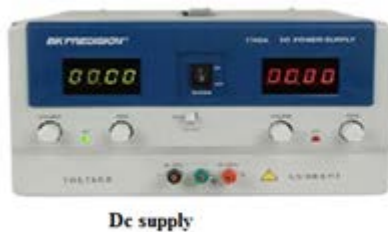
Experiment 8

Thyristors

Objectives:

In this experiment you are expected:
- To experimentally deal with SCR.
- To experimentally deal with TRIAC.

Apparatus:

Dc supply

Digital multimeter

Theoretical Background:

The Thyristor is a multi-layer semiconductor device that is used mainly as AC switches in AC power circuits, it is similar to the transistor. It requires a gate signal to turn it "ON", the "controlled" part of the name and once "ON" it behaves like a rectifying diode, the "rectifier" part of the name. In fact the circuit symbol for the thyristor suggests that this device acts like a controlled rectifying diode.

Examples on Thyristors:
1. SCR (Silicon Controlled Rectifier) Thyristor. See Figure 8.1.
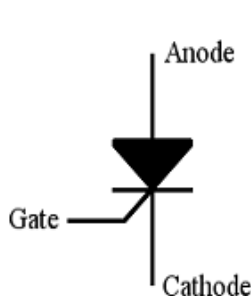2. Diac. See Figure 8.2.
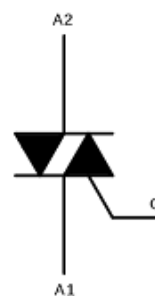3. Triac. See Figure 8.3.

Figure 8.1   Figure 8.2   Figure 8.3

- SCR (silicon controlled rectifier): is a special type of diode that only allows current to flow when a control voltage is applied to it's gate terminal. Although this appears to be nothing more than a voltage controlled switch the following should be noted: In the presence of forward current (i.e. after the thyristor is turned on by a suitable gate voltage) it will not turn off even after the gate voltage has been removed. The thyristor will only turn off when the forward current drops to zero. In a DC (Direct current) circuit this makes the device almost useless except in certain particular safety (crowbar) protection applications.

- Diac (Diode Alternating Current) is a full-wave or bi-directional semiconductor switch that can be turned on in both forward and reverse polarities, it is widely used to assist even triggering of a TRIAC when used in AC switches. DIACs are mainly used in dimmer applications and also in starter circuits for florescent lamps.

- The TRIAC (Triode for Alternating Current) is a three terminal semiconductor device for controlling current, it is effectively a development of the SCR or thyristor, but unlike the thyristor which is only able to conduct in one direction, the TRIAC is a bidirectional device.

Procedure:

Part1: SCR (BT151)
1. Construct the circuit shown in Figure 8.4
2. Switch on the power supply.
3. Increase V1 slowly from 0V to 12 V
4. Keep the power supply on (12V),and Close the switch J1 while the gate voltage is zero ,what happen?
5. Increase the gate voltage slowly till the led will be on. What is the Voltage at this moment? Calculate the needed current?
6. Open the switch J1, Write your observation.
7. How can you reset the thyristor?
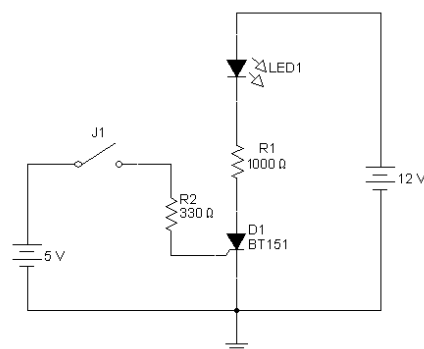8. Decrease the Supply voltage from 12V slowly, what is the minimum voltage for working.

Figure 8.4

Discussion and Analysis:

1- In step 3 (procedure), Is the LED turn on?, why.

2- while you Increasing the gate voltage slowly ,What is the Voltage at switching? Calculate the needed current?